**EXPERIMENT – 1**

**Dt- 21/09/2020**

**Aim of the experiment:**

Verification of all Logic Gates and implementation of logic gates ­using universal gates.

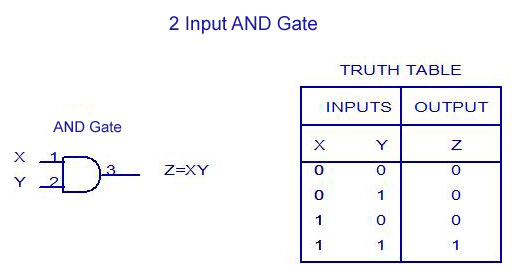
**Apparatus Required:**

* Tinkercad software
* Breadboard
* Switches
* LED
* Resistor – 1Kohm
* Power Supply
* IC of specific gate
* Connecting wires

**Theory:**

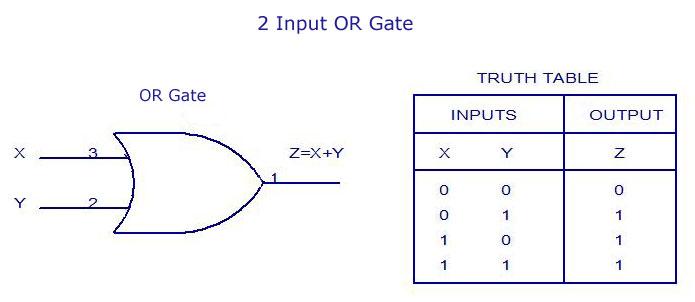
**AND GATE**

An AND gate requires two or more inputs and produce only one output. The AND gate produces an output of logic 1 state when each of the inputs are at logic 1 state and also produces an output of logic 0 state even if any of its inputs are at logic 0 state. The symbol for AND operation is ‘.’, or we use no symbol for representing.



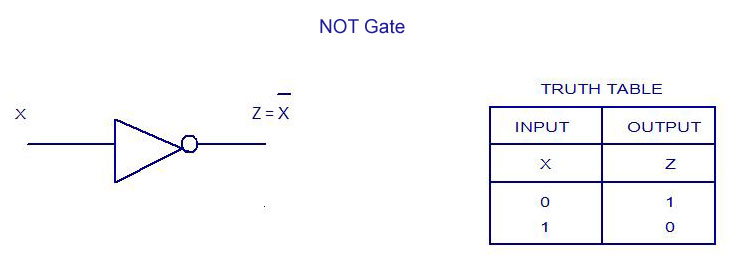
**OR GATE**

Similar to AND gate, an OR gate may also have two or more inputs but produce only one output. The OR gate produces an output of logic 1 state even if any of its inputs is in logic 1 state and also produces an output of logic 0 state if any of its inputs is in logic 0 state. The symbol for OR operation is ‘+’.



**NOT GATE**

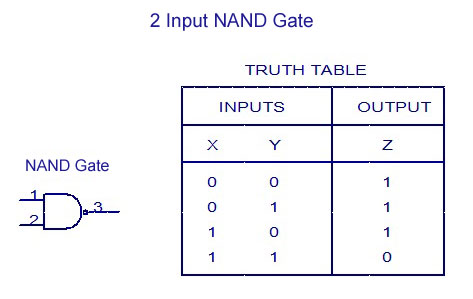
The NOT gate is also called as an inverter, simply because it changes the input to its opposite. The NOT gate is having only one input and one corresponding output. It is a device whose output is always the compliment of the given input. That means, the NOT gate produces an output of logic 1 state when the input is of logic 0 state and also produce the output of logic 0 state when the input is of logic 1 state. The NOT operation is denoted by’- ‘(bar).



**NAND GATE**

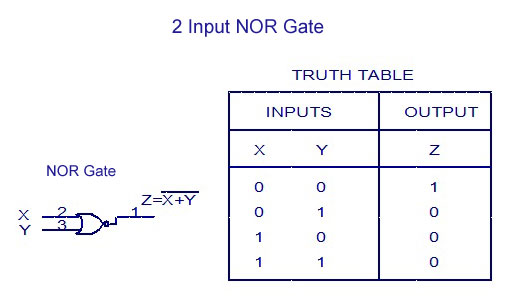
The NAND and NOR gates are the universal gates. Each of this gate can realize the logic circuits single handed. The NAND and NOR are also called as universal building blocks. Both NAND and NOR has the ability to perform three basic logic functions such as AND, OR and NOT. NAND gate is a combination of an AND gate and a NOT gate. The expression for the NAND

gate is ‘— ‘whole bar.



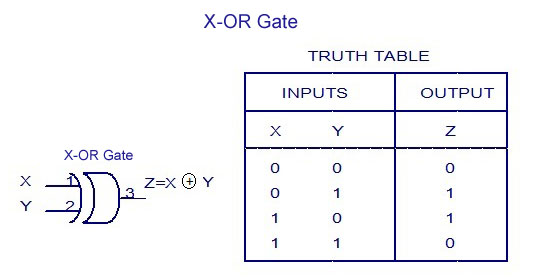
**NOR GATE**

NOR means NOT OR. That means, NOR gate is a combination of an OR gate and a NOT gate. The output is logic 1 level, only when each of its inputs assumes a logic 0 level. For any other combination of inputs, the output is a logic 0 level.



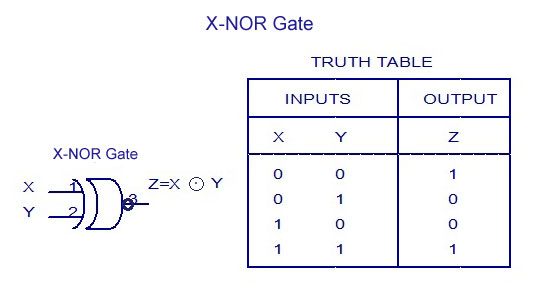
**EXCLUSIVE-OR GATE (X-OR) GATE**

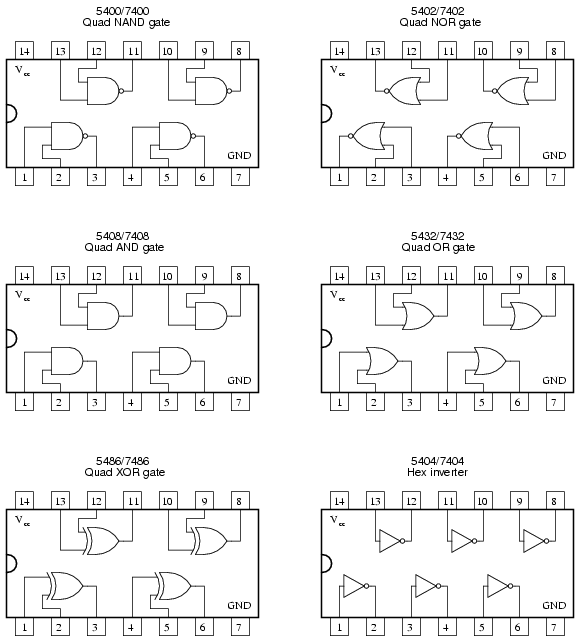
An X-OR gate is a two input, one output logic circuit. X-OR gate assumes logic 1 state when any of its two inputs assumes a logic 1 state. When both the inputs assume the logic 0 state or when both the inputs assume the logic 1 state, the output assumes a logic 0 state. The output of the X-OR gate will be the sum of the modulo sum of its inputs.



**EXCLUSIVE-NOR (X-NOR) GATE**

An X-NOR gate is a combination of an X-OR gate and a NOT gate. The X-NOR gate is also a two input, one output concept. The output of the X-NOR gate will be logic 1 state when both the inputs assume a 0 state or when both the inputs assume a 1 state. The output of the X-NOR gate will be logic 0 state when one of the inputs assume a 0 state and the other a 1 state.





***Procedure*** :-

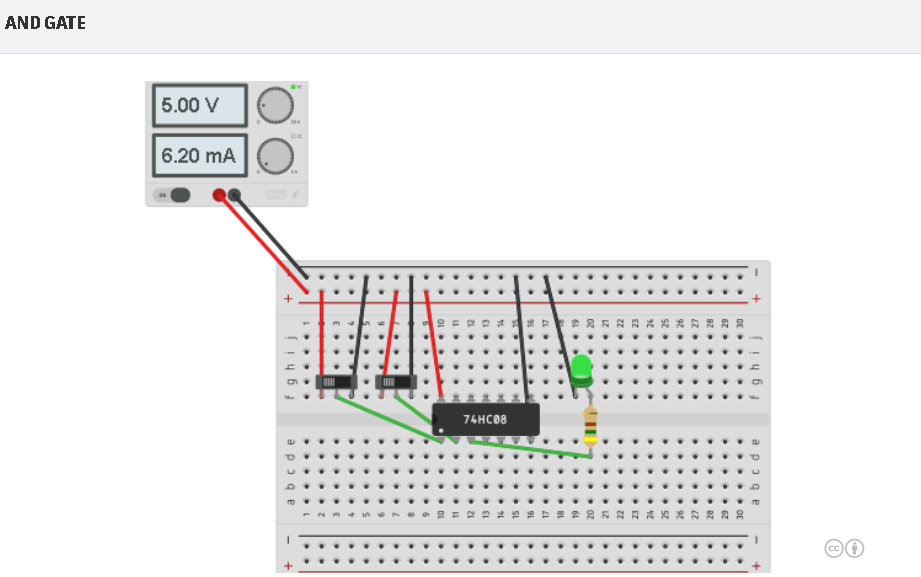
* Open Tinkercad Software and click on design new circuit.
* A new window opens, on the right hand tab, there are required materials for constructing a circuit. Select All for all required components for designing circuits.
* All required components are selected and circuit is designed.
* On the top right bar, after designing a circuit , start simulation button is clicked to start simulation.
* In simulation, all circuits are checked by manipulating signals by using slideswitches. Slideswitches can be ON or OFF which are equal to 1 or 0 input to gates.
* After verifying all inputs, select stop simulation.
* Similarly all given circuits are designed and tested.

From the given circuits designed, all inputs are tried and output signals are verified.

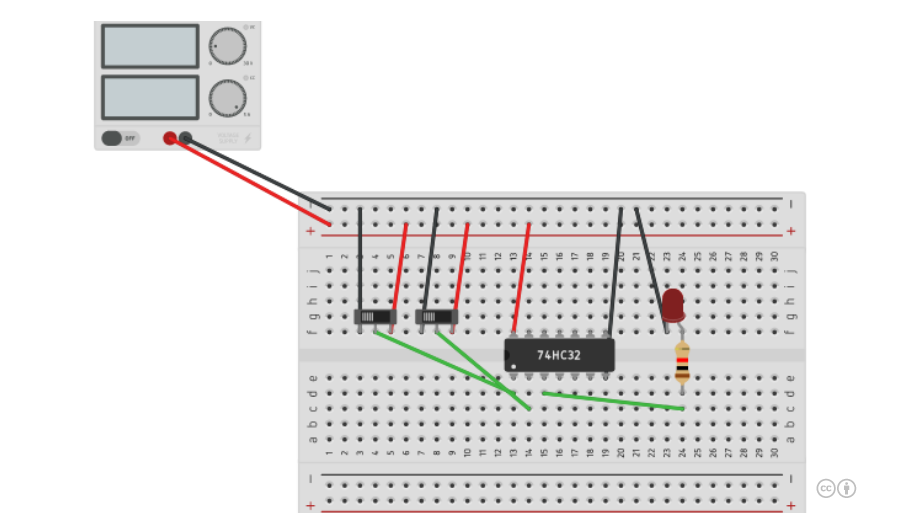
The various circuits designed are given below

**OBSERVATIONS:**

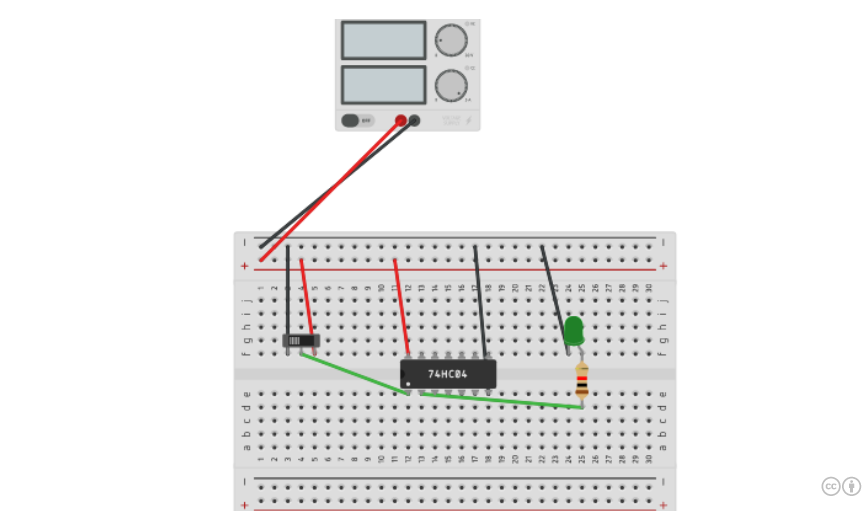
**AND GATE**

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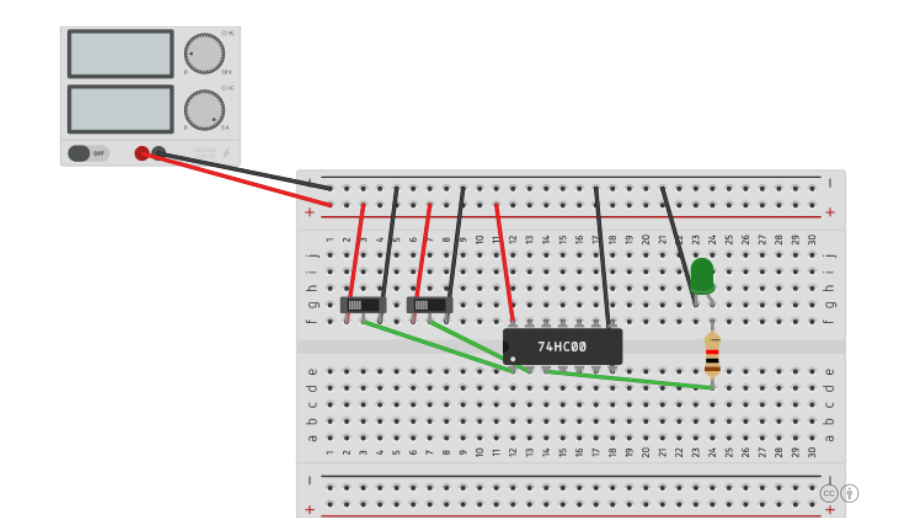
**OR GATE**

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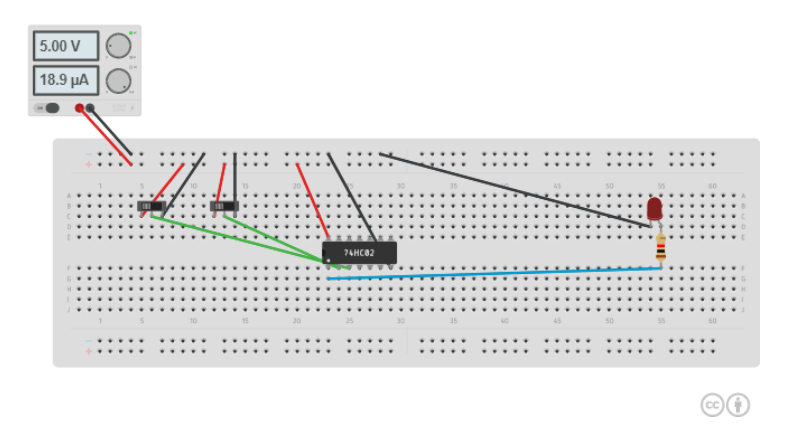
**NOT GATE**

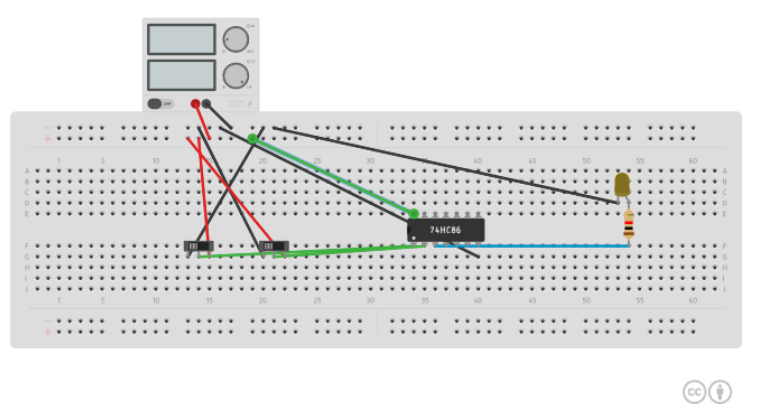


**NAND GATE**

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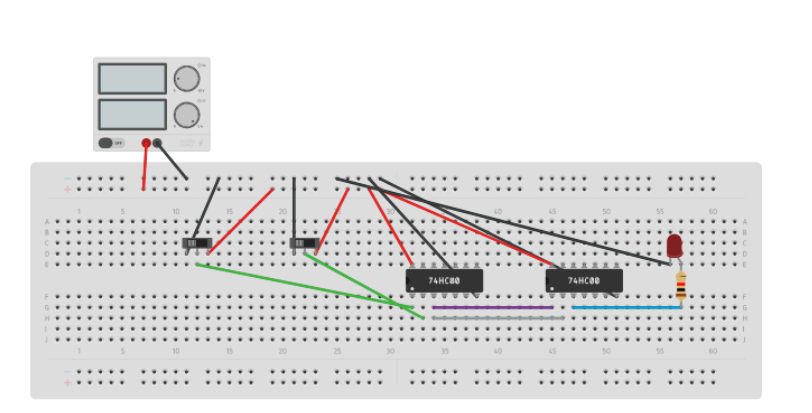
**NOR GATE**



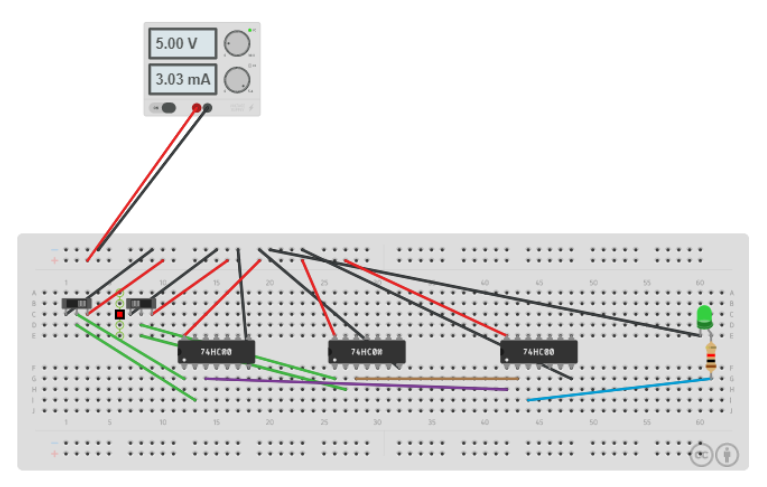
**EXCLUSIVE-OR GATE (X-OR) GATE**

**REALIZATION USING NAND GATE:**

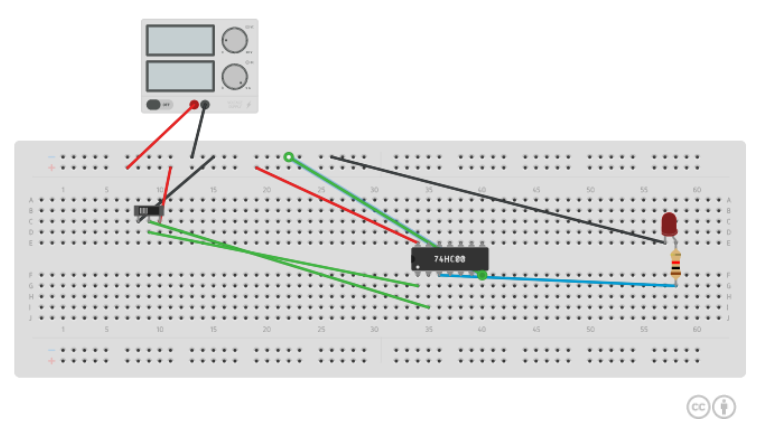
**AND GATE**



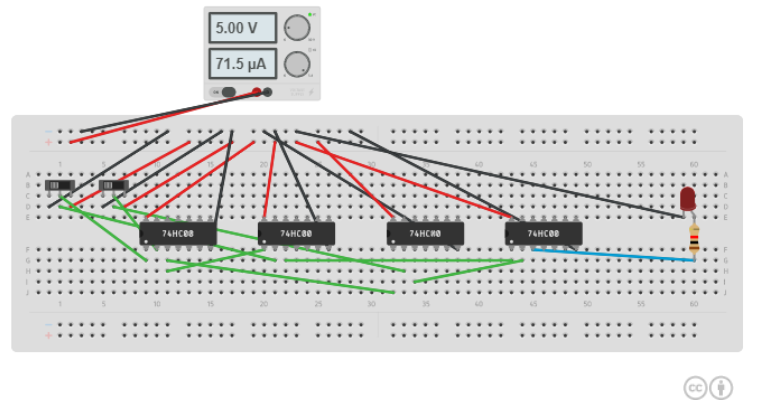
**OR GATE**



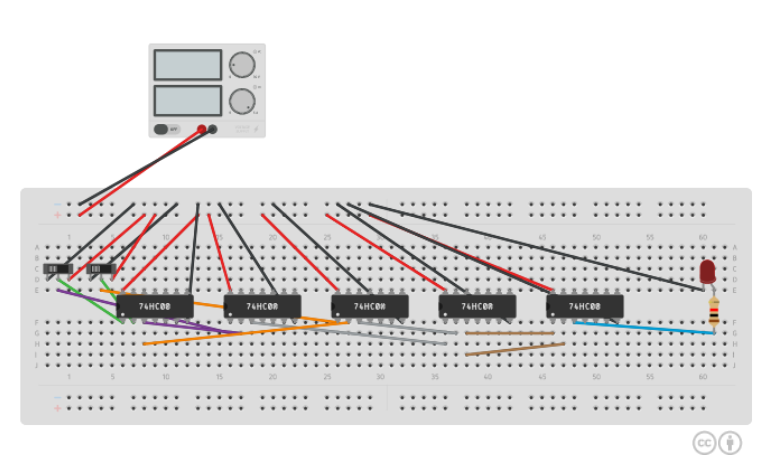
**NOT GATE**



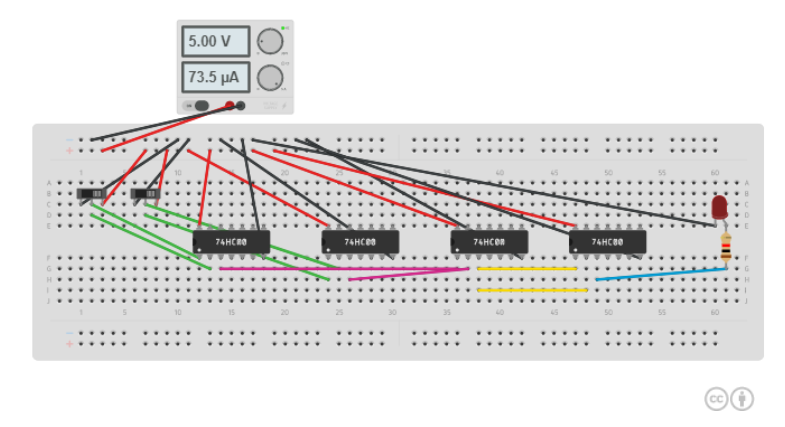
**XOR GATE**



**XNOR GATE**

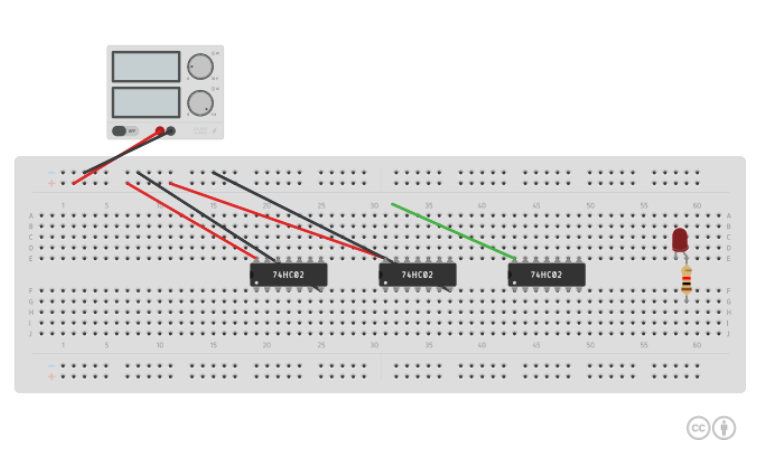


**NOR GATE**

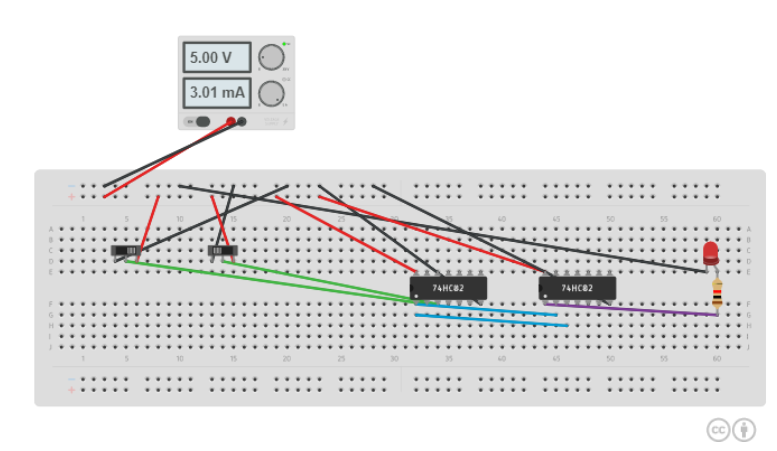


**REALIZATION USING NOR GATE:**

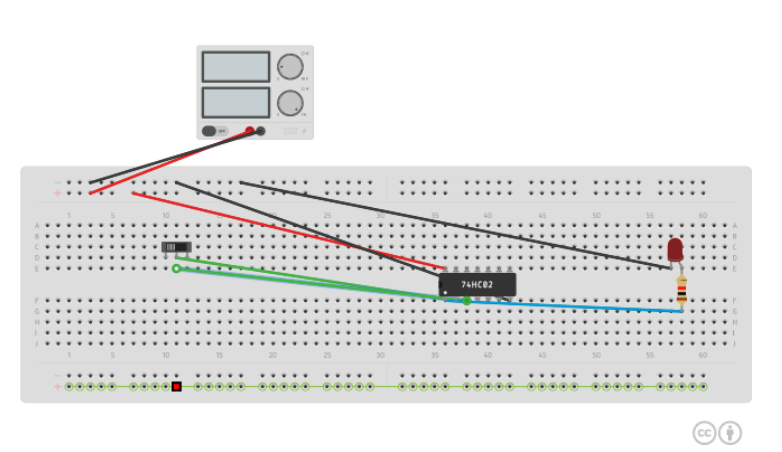
**AND GATE**



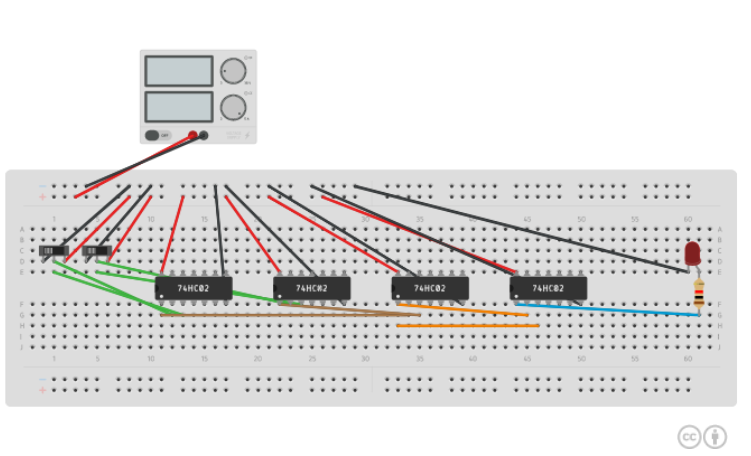
**OR GATE**



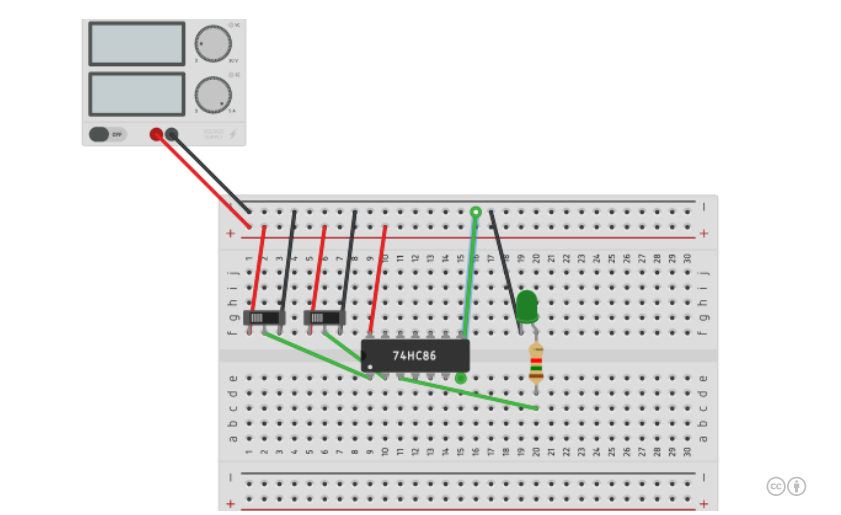
**NOT GATE**



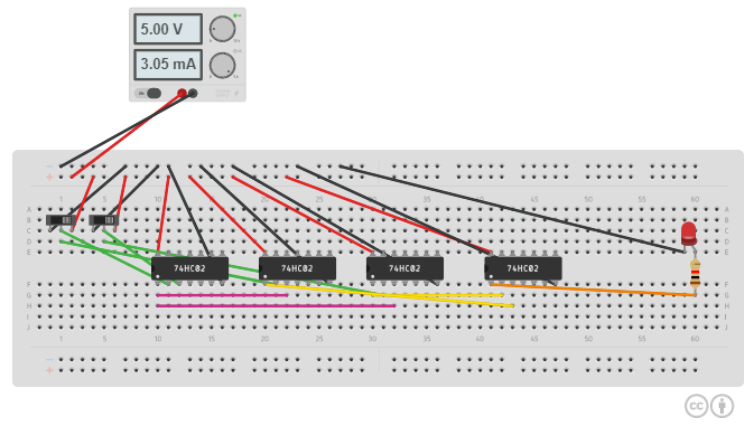
**NAND GATE**



**XOR GATE**



**XNOR GATE**



**Conclusion:**

Hence, I have successfully observed and performed all the experiments given in class.

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